Intel® 82804AA Memory Repeater Hub for SDRAM (MRH-S)

Datasheet

November 1999

Order Number: 298024-001

Datasheet

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Revision History

Rev.	Draft/Changes	Date
-001	• Initial Release	November 1999

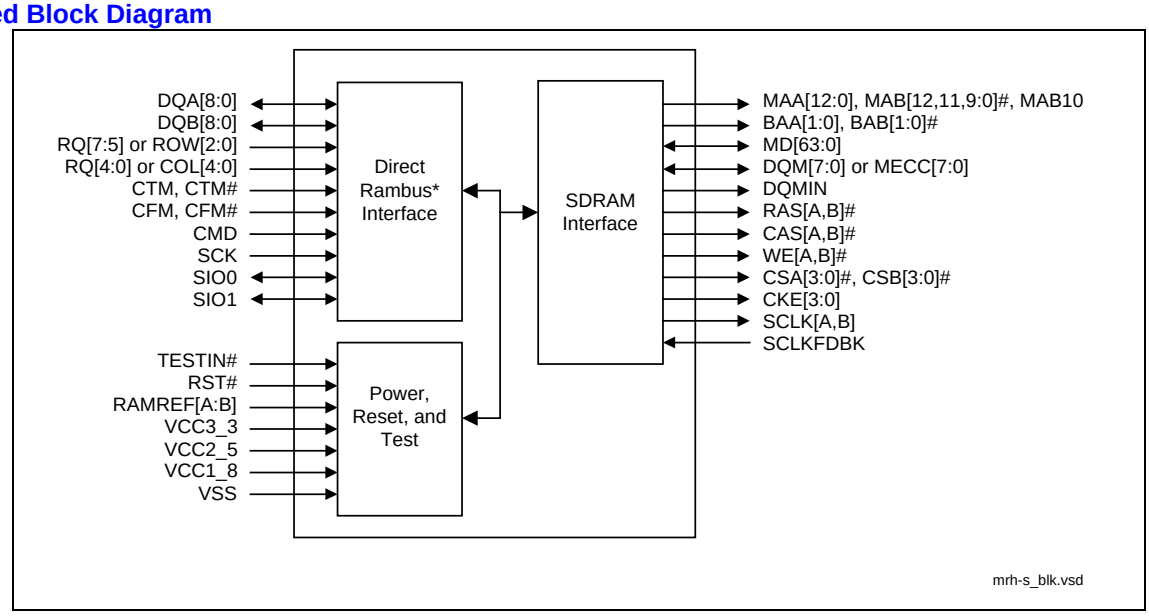
Intel® 82804AA MRH-S

Product Features

- 100 MHz SDRAMs on DIMMs
- 64Mbit, 128Mbit and 256Mbit SDRAM technologies
- x4, x8 and x16 SDRAM components
- Both registered and unbuffered ECC and Non-ECC DIMMs supported
- 3.3V I/O for SDRAM
- 400 MHz Direct RDRAM* Channel onl
- Maximum of 4 SDRAM rows per MRH-S. All rows share the same SDRAM data bus.
- 2 copies of the command and address signals to enhance electrical performance
- Write buffer to support modified Direct RDRAM write protocol
- Maximum of 2 MRH-S components on a single Direct RDRAM channel
- Interleaved operation supported for 2 MRH-S components on a single Direct RDRAM channel
- Support Self Refresh Low Power state of SDRAMs
- 2 clocks generated for SDRAMs and a feedback input for phase alignment
- Supports “1 Cycle” and “2 Cycle” command timing rules
- Direct RDRAM channel Current Calibration, Temperature Calibration and Levelization support
- Support of Direct RDRAM Channel CMOS signals to facilitate initialization and read/write of registers.
- 241-pin miniBGA

The Intel® 82804AA Memory Repeater Hub for SDRAM (MRH-S) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Simplified Block Diagram



1. Overview

1.1. System Architecture

The Intel® 82804AA MRH-S component supports SDRAM memory on a Direct RDRAM* Channel. The MRH-S has a Direct RDRAM interface that connects the Memory Controller Hub (MCH) and the MRH-S. The MRH-S also has an SDRAM interface that can support up to 4 SDRAM rows using two DIMMs.

1.2. Terminology

RAMBUS*

RSL	Rambus* Signaling Level is the name of the signaling technology used by Rambus*.
Rclk	Rclk refers to the RSL bus' high speed clock in a generic fashion, often in the context of clock counts in timing specifications.
RAC	Rambus* ASIC Cell. It is the embedded cell designed by Rambus* that interfaces with the Rambus* devices using RSL signaling.
RMC	Rambus* Memory Controller. This is the logic that directly interfaces to the RAC.
RIMM	Rambus* Interface Memory Module.
MCP	Memory Controller Packet. These packets contain the commands for the Direct RDRAM* Channel. The packets initiate Direct RDRAM reads and writes.

Components

MCH	The Memory Controller Hub component that contains the processor interface, RDRAM controller, and AGP interface. It communicates with the ICH over a proprietary interconnect called "Hub Interface".
82804AA MRH-S	The Memory Repeater Hub for SDRAM.
Direct RDRAM Channel	The RSL bus that connects the Memory Controller Hub to the MRH-S.
SDRAM Interface	The MRH-S interface to SDRAM DIMMs.

1.3. Supported Memory Configurations

The MRH-S supports 64Mbit, 128Mbit and 256Mbit SDRAM memory technologies. Table 1 displays the memory configurations supported by the MRH-S.

Table 1. SDRAM Configurations

Tech.	Config.	# of Row Addrs Bits	# of Col Addrs Bits	# of Bank Addrs Bits	Page size	DIMM Type
64 Mbit	16M x 4	12	10	2	8KB	Registered ONLY
	8M x 8	12	9	2	4KB	Registered and Unbuffered
	4M x 16	12	8	2	2KB	Unbuffered
128 Mbit	32M x 4	12	11	2	16KB	Registered ONLY
	16M x 8	12	10	2	8K	Registered and Unbuffered
256 Mbit	64M x 4	13	11	2	16KB	Registered ONLY
	32M x 8	13	10	2	8KB	Registered and Unbuffered

1.4. Maximum Memory Supported

Assumptions: Each MRH-S drives up to 2 DIMMs
Up to two MRH-Ss per Direct RDRAM* channel
Single Sided DIMM uses one SDRAM row (SS = Single Sides)
Double Sided DIMM uses two SDRAM row (DS = Double Sides)
Max memory based on the SDRAM configurations in Table 2 (except 64Mbit x16)

Table 2. Maximum Memory Support with DIMMs for Server/Workstation Platforms (1–4 DIMMs)

DRAM Configuration		1 DIMM		2 DIMMs		3 DIMMs		4 DIMMs	
		1 Row	2 Row	1 Row	2 Row	1 Row	2 Row	1 Row	2 Row
64Mb	x4	128	256	256	512	384	768	512	1024
	x8	64	128	128	256	192	384	256	512
128Mb	x4	256	512	512	1024	768	1536	1024	2048
	x8	128	256	256	512	384	768	512	1024
256Mb	x4	512	1024	1024	2048	1536	3072	2048	4096
	x8	256	512	512	1024	768	1536	1024	2048

NOTES: Maximum memory indicated in table is in MBs.

Table 3. Maximum Memory Support with DIMMs for Server/Workstation Platforms (5–8 DIMMs)

DRAM Configuration		5 DIMMs		6 DIMMs		7 DIMMs		8 DIMMs	
		1 Row	2 Row	1 Row	2 Row	1 Row	2 Row	1 Row	2 Row
64Mb	x4	640	1280	768	1536	896	1792	1024	2048
	x8	320	640	384	768	448	896	512	1024
128Mb	x4	1280	2560	1536	3072	1792	3584	2048	4096
	x8	640	1280	768	1536	896	1792	1024	2048
256Mb	x4	2560	5120	3072	6144	3584	7168	4096	8192
	x8	1280	2560	1536	3072	1792	3584	2048	4096

NOTES: Maximum memory indicated in table is in MBs.

1.5. System Interconnections

As an example, the 82840 MCH supports one or two MRH-Ss on each of its Direct RDRAM* channel buses for a maximum of four 82803AA MRH-Ss in an Intel® 840 chipset system memory array.

Note: Future Intel chipsets will support the MRH-Ss as well.

Figure 1 and Figure 2 show the 82840 MCH memory subsystem interconnections using the 82803AA MRH-S. Figure 3 shows the SDRAM data and address interconnections for an Unbuffered DIMM memory configuration. For information on unbuffered DIMMs or registered DIMMs, refer to the *PC SDRAM Unbuffered SDRAM Specification* or the *PC SDRAM Registered DIMM Specifications* located on the Intel Website.

Figure 1. 82840 Memory Subsystem using Two MRH-Ss

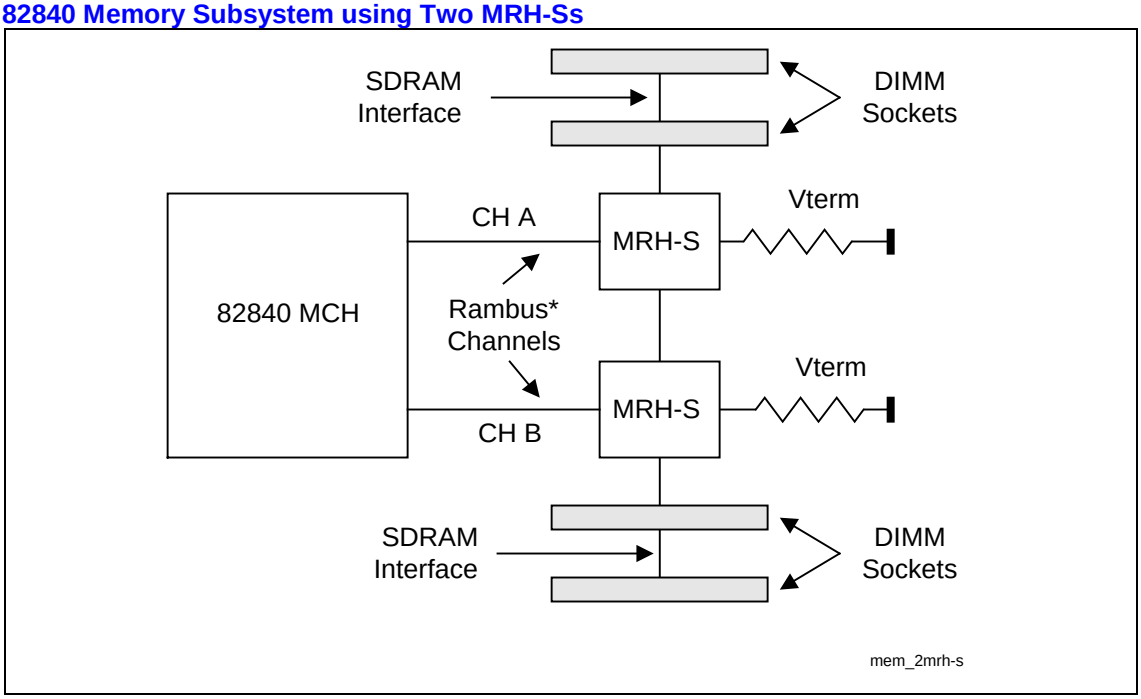


Figure 2. 82840 MCH Memory Subsystem using Four MRH-Ss

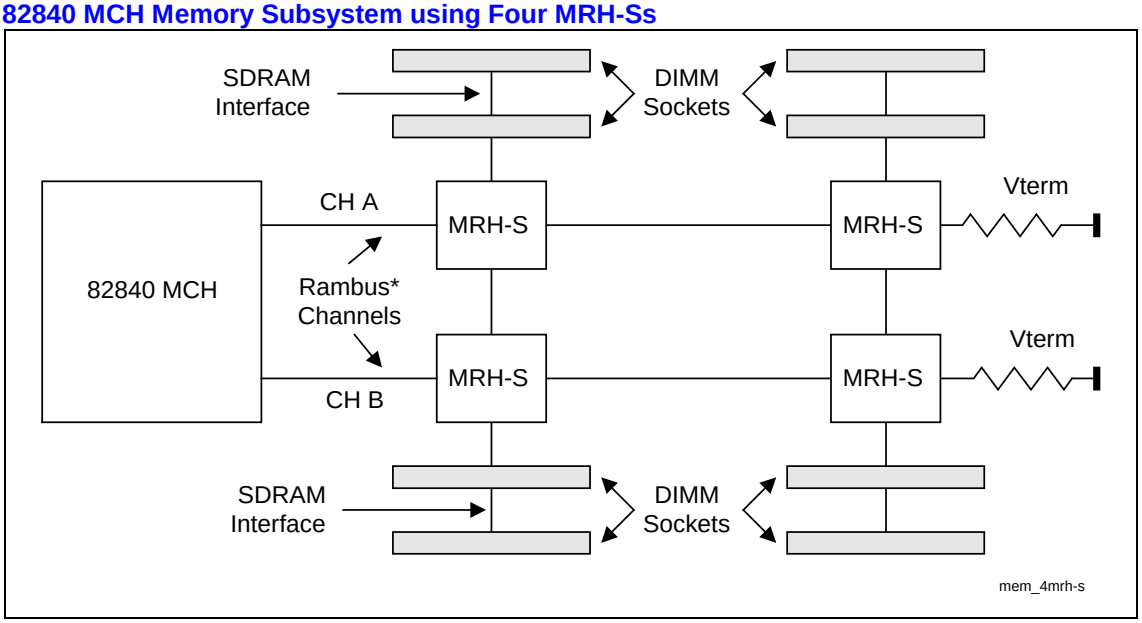
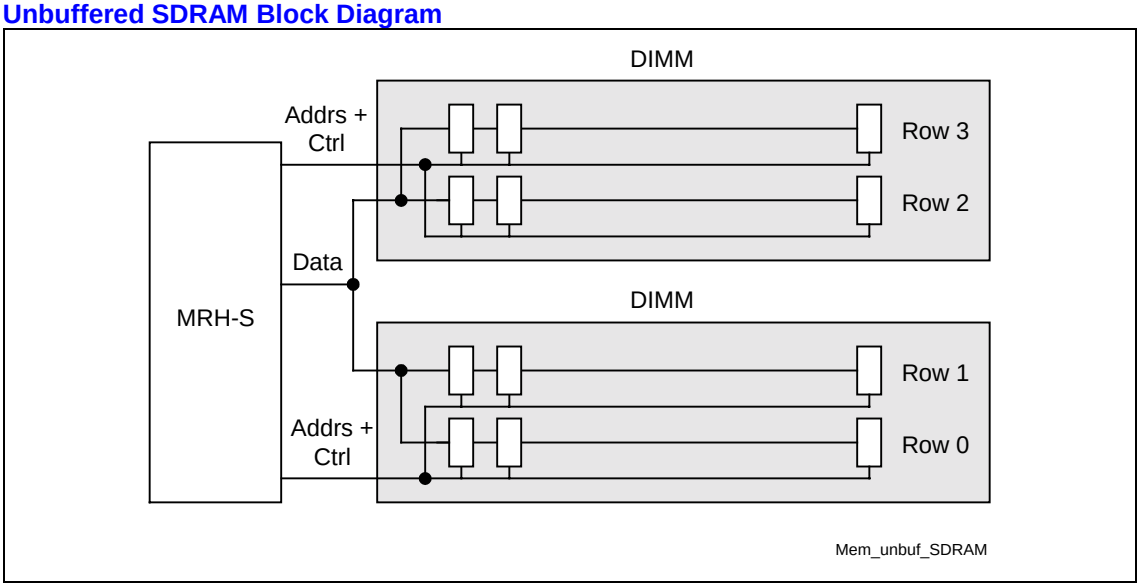


Figure 3: Unbuffered SDRAM Block Diagram



1.6. Direct RDRAM* Channel Interface

The Direct RDRAM* channel interface is the interconnection between the MCH and MRH-S. The Direct RDRAM channel interface consists of 30 RSL (4 Clocks) and 3 CMOS signals. The MRH-S supports the following Direct RDRAM, SDRAM, and host clock frequency combinations.

Table 4. Frequency Configurations

RDRAM* Frequency (MHz)	SDRAM Frequency (MHz)	Host Bus Frequency (MHz)
400	100	100
400	100	133

1.7. SDRAM Interface

The MRH-S supports up to four 64/72bit wide rows of SDRAM. Two copies of MA, BA, RAS#, CAS# and WE# signals are provided. Also 8 (two per row) copies of CS# and four copies (1 per row) of CKE signals are provided.

1.8. Clock Interface

The MRH-S provides two copies of the SDRAM clock source to be used with an external clock buffer for use with DIMMs. A clock feedback input is provided on the MRH-S to phase align the SCLK with the external clocks generated by the clock buffer.

1.9. Register Interface

The MRH-S has internal configuration and control registers. These registers are accessed through the SCK, CMD, and SIO CMOS signal interface.

2. Signal Description

The following notations are used to describe the signal types and their drive state:

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

RSL RDRAM* Signaling Level interface signal.

CMOS CMOS buffers.

2.1. Direct RDRAM* Channel Interface

Signal	Type	Description
DQA[8:0]	I/O RSL	**Data Bus, Data Byte A:** Bi-directional 9 bit data bus A. These signals correspond to the DQA[8:0] signals on the Direct RDRAM* channel.
DQB[8:0]	I/O RSL	**Data Bus, Data Byte B:** Bi-directional 9 bit data bus B. These signals correspond to the DQB[8:0] signals on the Direct RDRAM channel.
RQ[7:5]/ ROW[2:0]	I RSL	**Row Request Control:** These signals carry the section of the memory control packets (MCP) from the MCH to the MRH-S that control row accesses.
RQ[4:0]/ COL[4:0]	I RSL	**Column Request Control:** These signals carry the section of the memory control packets (MCP) from the MCH to the MRH-S that control column accesses.
SIO0	I/O CMOS 1.8V	**Serial I/O Chain Input:** This serial input/output pin is used for reading and writing control registers. This pin corresponds to the SIO signals on the Direct RDRAM channel. See Figure 4 for more information.
SIO1	I/O CMOS 1.8V	**Serial IO Chain Output:** This bi-directional signal is used to carry data for SIO operations: register access, MRH-S reset, and MRH-S ID initialization. This pin corresponds to the SIO0 signal of the next MRH-S on the Direct RDRAM channel. See Figure 4 for more information.
SCK	I CMOS 1.8V	**Serial Clock:** Clock source used for timing of the SIO and CMD signals. This corresponds to the SCK signal on the Direct RDRAM channel.
CMD	I CMOS 1.8V	**Serial Command:** Serial command input used for control register read and write operations. This corresponds to the CMD signal on the Direct RDRAM Channel.
CTM	I RSL	**Clock To MCH:** One of the two differential transmit clock signals used for MRH-S to MCH operations.
CTM#	I RSL	**Clock To MCH Complement:** One of the two differential transmit clock signals used for MRH-S to MCH operations.
CFM	I RSL	**Clock From MCH:** One of the differential receive clock signals used for MCH to MRH-S operations.
CFM#	I RSL	**Clock From MCH Complement:** One of the differential receive clock signals used for MCH to MRH-S operations.

2.2. SDRAM Interface

Signal	Type	Description
MAA[12:0] MAB[12:11,9:0]#, MAB10	O CMOS 3.3V	**SDRAM Memory Address:** Used for providing multiplexed row and column address to SDRAM. There are two sets of MA signals (MAA and MAB). Each set can drive up to two rows of SDRAM. The MAB [12:11, 9:0] are inverted copies of MAA[12:11, 9:0]. MAA10 and MAB10 are identical copies.
BAA[1:0] BAB[1:0]#	O CMOS 3.3V	**SDRAM Bank Address:** Used for providing bank address to SDRAM. There are two sets of BA signals (BAA and BAB). Each set can drive up to two rows of SDRAM. BAB [1:0] are inverted copies of BAA[1:0].
MD[63:0]	I/O CMOS 3.3V	**SDRAM Data:** These signals are used to interface with the SDRAM data bus.
DQM[7:0] or MECC[7:0]	O CMOS I/O CMOS 3.3V	**SDRAM Data Mask:** These signals are available as SDRAM byte enables for write data in systems that do not support ECC. **Memory ECC Data:** These signals are available as ECC data during write operation in systems which support ECC. When ECC is supported, all writes are read-modify-writes and, hence, the DQM signals of the SDRAM devices can be tied to logic zero.
DQMIN	O CMOS 3.3V	**DQM Input (SDRAM input):** This signal is only used when the MRH-S is in ECC mode. In ECC mode, this pin must be connected to all DQM pins of the SDRAMs. After the power up of the MRH-S, this signal is driven high until the SDRAM initialization done (SID) bit in the MOR register is set to 1. When SID is 1, this signal is driven to 0. Not used with DQM[7:0] signals routed
RASA# RASB#	O CMOS 3.3V	**SDRAM Row Address Strobe:** These signals are used to latch the row and bank addresses on the MAxx and BAxx lines into SDRAM. Each signal can drive up to two SDRAM rows.
CASA# CASB#	O CMOS 3.3V	**SDRAM Column Address Strobe:** These signals are used to latch the column and bank addresses on the MAxx and BAxx lines into SDRAM. Each signal can drive up to two SDRAM rows.
WEA# WEB#	O CMOS 3.3V	**SDRAM Write Enable:** These signals are used for write and pre-charge operations to SDRAM. Each signal can drive up to 2 SDRAM rows.
CSA[3:0]# CSB[3:0]#	O CMOS 3.3V	**SDRAM Chip Select:** These signals are used for selecting the SDRAM row. There are two copies of this signal for each SDRAM row (CSA is a copy of CSB. CSA/B[0] activates SDRAM row 0. CSA/B[1] activate SDRAM row 1. CSA/B[2] activate SDRAM row 2. CSA/B[3] activate SDRAM row 3.).
CKE[3:0]	O CMOS 3.3V	**SDRAM Clock Enable:** These signals are used for signaling powerdown entry, powerdown exit, self refresh entry and self refresh exit commands to an SDRAM row. There is one CKE signal per row, CKE0 for row 0, CKE1 for Row 1, CKE2 for Row 2 and CKE3 for Row 3.
SCLKA SCLKB	O CMOS 3.3V	**SDRAM Clocks:** Two copies of the SDRAM clock are generated by the MRH-S. External buffers are required to generate an adequate number of clocks required by DIMMs.
SCLKFDBK	I CMOS 3.3V	**SDRAM Clock Feedback:** Feedback reference from the external SDRAM clock buffer. This clock is used by the MRH-S when writing and reading data to/from the SDRAM array.

2.3. Miscellaneous Signals Interface

2.3.1. Reset and Miscellaneous

Signal	Type	Description
TESTIN#	I CMOS 3.3V	**Test Input:** This pin is used for manufacturing and board level test purposes. TESTIN# is sampled on the rising edge of RST#.
RST#	I CMOS 3.3V	**Reset:** This signal is used for resetting the internal logic during power up. This signal must not be asserted during STR exit.

2.3.2. Reference Pins

Signal	Description
RAMREF[A:B]	**RDRAM* Reference:** Reference voltage input for the RDRAM RSL interface.
VCC3_3	**3.3V Power:** Power pins for SDRAM interface.
VCC2_5	**2.5V Power:** Power pins for core.
VCC1_8	**1.8V Power:** Power pins for RDRAM interface.
VSS	**Ground**

3. Register Description

3.1. MDID—Device ID Register

Address: 02h
Default: 0030h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:6	Reserved
5:4	**Device ID Select.** 00 = Reserved 10 = Reserved 01 = Reserved 11 = The Device ID[3:2] in the MCP packet is compared against the Device ID[3:2] to identify the selected MRH-S. The Device ID[1:0] of the MCP packet is used to identify the selected SDRAM row. All four SDRAM rows of the MRH-S can be used.
3:0	**Device ID:** This field specifies the device ID of the MRH-S. This field is compared against the Device ID field of the MCP packet to determine if this is the addressed MRH-S device.

3.2. MTR—Timing Register

Address: 03h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15	Reserved
14	**SCLKB Disable:** 1 = Disable. the SCLKB output pin is disabled 0 = Enable.
13	**ECC Mode Enable:** 1 = Enable. ECC mode of operation is enabled. The MRH-S just passes the ECC code it received through the data packet to the SDRAM interface. It does not check the ECC code for errors. In ECC mode byte masking is not supported. 0 = Disable. MRH-S does not support ECC. In non-ECC mode the DQM signals are used for byte masking.

Bit	Descriptions
12	**MRH-S Disable:** 1 = Disable. MRH-S is functionally disabled. The MRH-S will not monitor the input signals nor will it drive output signals. When the MRH-S is disabled, its serial interface signals (SIO0, SIO1, CMD and SCK) do function as normal. After power up the MRH-S is in disabled mode. A reset (RST# active) has to be applied to the MRH-S to get it out of the disabled mode. 0 = Enable.
11:10	Reserved.
9	**Registered DIMM Timing Enable (RDTE):** 1 = Enable. Registered DIMM timings are assumed for SDRAM operation. This means that CL=2 is interpreted as CL=3 and CL=3 is interpreted as CL=4. Also the write data has to be sent one cycle later than unbuffered SDRAM. 0 = Disable.
8	**Relaxed SDRAM Timing Enable (RSTE):** 1 = Enable. Two cycle rule for accessing the SDRAM is employed. The two cycle rule defines that the MAx and the other control signals (RAS, CAS, WE and DQM) for SDRAM are driven one cycle before CS# is applied. 0 = Disable. MAx and other control signals are asserted along with CS# for one cycle duration.
7:6	Reserved
5:4	**TCAC:** This field defines the minimum delay from read command to read data on the Direct RDRAM channel. The tCAC value is dependent on the value of the RSTE bit. TCAC is in RDRAM channel clocks. **Bit[5:4] RSTE = 0 RSTE = 1** 00 21 24 01 25 28 10 29 32 11 33 36
3	**CAS Latency (tCL):** This bit specifies the number of SCLKs between when a read command is sampled by the SDRAMs and when the samples read data from the SDRAMs. 0 = 2 SCLKs 1 = 3 SCLKs
2:0	**Direct RDRAM Channel Levelization Delay:** This field specifies the amount of levelization required in the MRH-S to levelize the read data going onto the Direct RDRAM channel. The delay is in Rclks. 000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7

3.3. MOR—Operation Register

Address: 04h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:9	Reserved
8	**SDRAM Initialization Done (SID):** 1 = Done. BIOS must set this bit to indicate the completion of SDRAM initialization. The inverted version of this bit drives the DQM pin. This bit has to be set to 1 by BIOS before it attempts to read or write the SDRAM memory. 0 = Not done
7	**Broadcast SDRAM Initialization Command (Broadcast SIC):** 1 = SIC command specified by bits [2:0] is issued to all four SDRAM rows. 0 = SIC command specified by bits [2:0] is issued only to the row specified by Row Select field (bits [4:3]).
6	**Mode Register Set (MRS) Field:** This bit defines the value of MAx[12:0] to be used with MRS command. Note that these values are the values seen by SDRAMs on their MAx[12:0] pins. 0 = 0031h 1 = 0021h
5	**Initiate SIC Operation (ISO):** When software sets this bit to 1, execution of the SIC command specified by bits[2:0] starts. After the execution is completed the MRH-S clears this bit to 0. Software must check to see if this bit is zero before writing to this bit. 1 = Start execution (execution in progress) 0 = Not started. (execution is not in progress)
4:3	**Row Select (RS):** Specifies the SDRAM row to be used with SIC field. 00 = Row 0 01 = Row 1 10 = Row 2 11 = Row 3
2:0	**SDRAM Initialization Command (SIC):** This field allows the MRH-S to issue various commands to the SDRAM row specified by bits [4:3]. BIOS uses this field to initialize the SDRAMs. BIOS programs this field with the appropriate command and sets bit 5 to 1. When the MRH-S sees bit 5 set to 1, it executes the command specified by the SIC field and at end of command execution sets bit 5 to 0. 000 = Reserved 001 = **NOP Command:** When the MRH-S receives this command it issues a NOP command to the SDRAM row specified by bits [4:3]. 010 = **All Banks Precharge:** When the MRH-S receives this command it issues an All Banks Precharge command to the SDRAM row specified by bits [4:3]. 011 = **Mode Register Set:** When the MRH-S receives this command it issues a Mode Register Set (MRS) command to the SDRAM row specified by bits [4:3]. Bit 6 of this register defines the value of A[12:0] to be used with this command. 100 = **Burst CAS before RAS (CBR):** When the MRH-S receives this command it issues eight CBR commands to the SDRAM row specified by bits [4:3].

3.4. MBSCRA—Memory Buffer Strength Control A Register

Address: 05h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:14	**MD[63:0]:** This field sets the buffer strengths for MD[63:0] pins. 00 = 1x 01 = 2x 10 = Reserved 11 = Reserved
13:12	**MECC[7:0]/DQM[7:0]:** This field sets the buffer strengths for MECC[7:0]/DQM[7:0] pins. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
11	**CSA0#/CSB0#:** This field sets the buffer strengths for CSA0#/CSB0# pins. 0 = 1x 1 = 2x
10	**CSA1#/CSB1#:** This field sets the buffer strengths for CSA1#/CSB1# pins. 0 = 1x 1 = 2x
9	**CSA2#/CSB2#:** This field sets the buffer strengths for CSA2#/CSB2# pins. 0 = 1x 1 = 2x
8	**CSA3#/CSB3#:** This field sets the buffer strengths for the CSA3#/CSB3# pins. 0 = 1x 1 = 2x
7:6	**CKE3:** This field sets the buffer strength for the CKE3 pin. 00 = 1x 01 = reserved 10 = 2x 11 = 3x
5:4	**CKE2:** This field sets the buffer strength for the CKE2 pin. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
3:2	**CKE1:** This field sets the buffer strength for the CKE1 pin. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
1:0	**CKE0:** This field sets the buffer strength for the CKE0 pin. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x

3.5. MBSCRB—Memory Buffer Strength Control B Register

Address: 06h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7:6	**MAA[12:0], BAA[1:0], RASA#, CASA#, WEA#:** This field sets the buffer strengths for MAA[12:0], BAA[1:0], RASA#, CASA# and WEA# pins. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
5:4	**MAB[12:11,9:0]# & MAB10, BAB[1:0]#, RASB#, CASB#, WEB#:** This field sets the buffer strengths for MAB[12:11,9:0] & MAB[10], BAB[1:0]#, RASB#, CASB# and WEB# pins. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
3:0	Reserved

3.6. EXCC—Direct RDRAM* Current Register

Address: 07h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:7	Reserved
6:0	**Current Control:** This 7-bit field controls the current for DQA[8:0] and DQB[8:0] RSL pins. For details, refer to *RDRAM Technical Specifications*.

3.7. RIR—RAC Initialization Register

Address: 09h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Ready for Synchronization Packet:** The MRH-S sets this bit when it is ready to accept the Synchronization MCP packet. The BIOS must check this bit before sending the Synchronization packet to the MRH-S. 1 = Ready 0 = Not Ready
4	**RAC Initialization Complete (RC):** The MRH-S sets this bit after it has completed RAC initialization. The BIOS must check this bit to make sure the RAC is properly initialized before initiating memory accesses. 1 = Complete 0 = Not complete
3	**Initiate RIC Operation (IRO):** When software sets this bit to 1, execution of the RIC command specified by bits[2:0] starts. After the execution is completed the MRH-S clears this bit to 0. The BIOS must check to see if this bit is zero before writing to this bit. 1 = Start execution (execution in progress) 0 = Complete
2:0	**RAC Initialization Command (RIC):** This field allows the BIOS to initialize the MRH-S RAC. The BIOS programs this field with the appropriate command and sets the IRO (bit[3]) to 1. When the MRH-S sees bit[3] set to 1, it executes the command specified by the RIC field and at the end of command execution sets bit[3] to 0. 000 = Reserved 001 = Initialize RAC: When receives this command it performs initialization sequence on the RAC. The initialization process includes executing the power up sequence to the RAC and Current and Temperature Calibrating of the RAC. 010 = Manual Current Calibrate the RAC: When receives this command it issues a manual Current Calibrate sequence to the RAC. The Current Control value specified in the EXCCA register is used as the manual current control value. 011 = Temperature Calibrate the RAC: When receives this command it issues a Temperature Calibrate sequence to the RAC. 100 = Reserved All other combinations reserved.

3.8. RAC Configuration Register A

Address: 0Ah
Default: 0000h
Access: Read/Write
Size: 16 Bits

Bits	Description
15:0	**RAC Configuration Bits [15:0]:** Reserved

3.9. RAC Configuration Register B

Address: 0Bh
Default: 0000h
Access: Read/Write
Size: 16 Bits

Bits	Description
15:11	**RAC Configuration Bits [31:27]:** Reserved
10	**RAC Coniguration Bits [26]:** On-die Termination Resistor Enable. 1 = Enable 0 = Disable
9:8	**RAC Configuration Bits [25:24]:** Early Clamp Enable. 00 = Disable 11 = Enable 01 or 10 = Reserved
7:0	**RAC Configuration Bits [23:16]:** Reserved

3.10. INIT—Initialization Register

Address: 21h
Default: 0009Fh
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7	**SIO Repeater bit (SRP):** This bit controls the value on the SIO1 pin. After an SIO Reset command is executed, the MRH-S sets SRP to 1. 1 = SIO1 = SIO0 0 = SIO1 = 1
6:5	Reserved

Bit	Descriptions
4:0	**Serial ID:** This field specifies Serial ID of the MRH-S. The serial ID is compared against the serial address in initialization request packets to determine if this is the addressed MRH-S device. The default value of Serial ID is 1Fh

3.11. VID—Vendor Identification Register

Address: 35h
Default: 8086h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:0	**Vendor Identification Number:** This is a 16 bit value assigned to Intel. Intel VID = 8086h.

3.12. RID—Revision Identification Register

Address: 36h
Default: 0000h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7:0	**Revision Identification Number:** This is an 8 bit field that identifies the revision identification number for the MRH-S. For A0 stepping this value is 10h.

3.13. DID—Device Identification Register

Address: 37h
Default: 2521h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:0	**Device Identification Number:** This is a 16 bit value assigned to the MRH-S.

4. Functional description

4.1. Operation Overview

When the MRH-S receives a command from the MCH, it decodes the command and drives the appropriate signals on the SDRAM interface. For read commands, the MRH-S receives data from the SDRAMs and then converts the data to the appropriate Direct RDRAM* packet format before sending it to the MCH. The MRH-S is aware of the CAS Latency (CL) for the SDRAMs and adjust the timings accordingly.

The MRH-S supports a modified version of RDRAM write protocol on the Direct RDRAM channel. To support it, the MRH-S contains a write buffer to temporarily store the write data and control from the MCH. The MRH-S stores this data to SDRAM after receiving a retire command (implied or explicit) from the MCH.

The MRH-S also supports the Current Calibration and Temperature Calibration of the Direct RDRAM channel after receiving the commands from the MCH.

The MRH-S contains registers for configuration and control. These registers are accessed through the CMOS interface provided by Direct RDRAM channel.

4.2. Protocol Overview

For the Direct RDRAM Channel, there are two groups of high speed RSL signals. These two groups are high speed RSL data and control bus signals. There is also a group of low speed CMOS control signals. The high speed control signals are referred to as the Request Control (RQ) and data signals are referred to as DQA and DQB. The Request Control signals carry the Memory Control Packets (MCP) from the MCH to the MRH-S.

4.2.1. Packet Format

A command packet uses all 8 RSL request signals (RQ[7:0]) on the channel to send the command from the MCH to the MRH-S. This command packet is known as MCP (Memory Control Packet). There are 32 bits in a MCP packet. The MCP packet is sent over the channel in two RDRAM clocks (RClks).

4.2.2. SDRAM Command Truth Table

Table 5 shows the SDRAM command encoding for the respective MCP commands.

Table 5. SDRAM Command Truth Table

Function	SCLK n	SCLK n-1	CKE n	CKE n-1	CS#	RAS#	CAS#	WE#	A11	A10	BA[1:0]	A[9:0]
NOP	R	R	H	x	L	H	H	H	x	x	x	x
Read	R	R	H	x	L	H	L	H	V	L	V	V
Read with autoprecharge	R	R	H	x	L	H	H	V	V	H	V	V
Write	R	R	H	x	L	H	L	L	V	L	V	V
Write with autoprecharge	R	R	H	x	L	H	L	L	V	H	V	V
Bank Activate	R	R	H	x	L	L	H	H	V	V	V	V
Precharge selected bank	R	R	H	x	L	L	H	L	V	L	x	x
Precharge all banks	R	R	H	x	L	L	H	L	x	H	x	x
Refresh	R	R	H	H	L	L	L	H	x	x	x	x
Self Refresh Entry	R	R	H	L	L	L	L	H	x	x	x	x
Self Refresh Exit	R	R	L	H	H	x	x	x	x	x	x	x
Mode Register Set	R	R	H	x	L	L	L	L	L	L	V	V
Clock Stop	R	L	x	x	x	x	x	x	x	x	x	x

NOTES:

1. x = Don't care, H = Logic high, L = Logic Low, R = Clock running, V = Valid address

4.2.3. Current Calibration

After receiving the Current Calibrate and Sample commands from the MCH, the MRH-S must initiate the current calibrate process of its Direct RDRAM interface. For details refer to the *RDRAM Technical Specifications*.

4.2.4. Temperature Calibration

After receiving the Temperature Calibrate command from the MCH, the MRH-S must initiate the temperature calibration process of its RAC. For details refer to *RDRAM Technical Specifications*.

4.2.5. SDRAM CBR Refresh

The MRH-S supports only CAS-before-RAS (CBR) refresh for active refresh. The MRH-S sends the CBR command to an SDRAM row when it receives the appropriate MCP from the MCH. Also, the MRH-S sends eight consecutive CBR commands (appropriately timed) to the specified SDRAM row after receiving a Burst CBR serial command through the MOR register.

4.2.6. Self Refresh Entry and Exit

The MRH-S supports self refresh entry and exit commands.

4.2.7. Registered DIMM Support

The MRH-S supports Registered DIMMs with CAS latencies of 2 or 3. Bit 9 of the MTR register must be set to 1 to enable the Registered DIMM operation. Also, the appropriate tCAC value must be programmed.

4.2.8. SDRAM Command Issue Rules

The MRH-S supports two timing modes for sending commands to SDRAM. These modes are known as “1 Cycle” and “2 Cycle” command timing rules.

- **“1 Cycle” Command Rule:** In this mode the control signals, MA, RAS#, CAS# and WE# are driven to an SDRAM row in the same clock (SCLK) that CS# is driven for that row.
- **“2 Cycle” Command Rule:** In this mode the control signals MA, RAS#, CAS#, and WE# are driven to an SDRAM row one clock (SCLK) earlier than the CS# is driven for that row.

4.2.9. Write Operation Policy

The MRH-S implements a modified version of RDRAM write protocol as described below. The MRH-S implements a write buffer that temporarily stores the write data, address, and control for up to two write commands from the MCH. A 16-byte data packet from the write buffer is sent to SDRAM when a retire command (explicit or implicit) is received by the MRH-S. If the retire command specifies masked retire, the mask bits in the retire command must be used as DQM signals for writes to the SDRAM.

The rules for write operation are:

- The write data will be sent two 1 or 2 (depending on Host bus frequency) Direct RDRAM channel clocks after the write MCP packet is sent.
- A MCP to retire the data, in the MRH-S, to SDRAM must be sent along with the data packet. One of the following MCPs will retire data to the SDRAM:
  - A retire MCP to the same MRH-S; or
  - A write MCP to a different MRH-S or a read MCP to a different MRH-S must be sent along with the data packet. This retires the data to SDRAM.

4.2.10. ECC Support

The MRH-S supports either ECC or non-ECC SDRAM DIMMs. The MRH-S supports ECC by passing the ECC code from the Direct RDRAM channel to SDRAM and vice versa. The MRH-S does not monitor the data for errors as it passes between the Direct RDRAM channel and the SDRAM array. If ECC-mode is enabled, byte masking is disabled.

4.2.11. SDRAM Initialization

The SDRAM initialization is performed in BIOS by programming the MOR register in the MRH-S. This register is accessed through the Direct RDRAM CMOS interface signals SCK, SIO, and CMD.

4.2.12. STR Support

The MRH-S supports the STR power management state by maintaining the appropriate states on the SDRAM interface signals. The system puts the MRH-S in the STR state by executing the following sequences:

- Issue Self Refresh entry commands to all SDRAM rows
- Issue Stop Clock command to MRH-Ss. (After receiving this command, the MRH-S powers down the RAC and turns off the SDRAM PLL. This turns off the SCLKs going to SDRAM rows.)
- Turn off the system clock generators.

The VCC power to the MRH-S must be maintained during STR. The following power sources must be kept alive to the MRH-S during STR:

- VCC2.5: Core
- VCC1.8: SCK, CMD and SIO interface
- VCC3.3: SDRAM interface

Note: The MRH-S RST# should NOT be toggled when entering or exiting STR (ACPI S3)

During STR exit, BIOS does the initialization of the MRH-S RAC after the RDRAM channel clock is stable. The initialization includes current and temperature calibration of the RAC. BIOS then issues a synchronization packet to the MRH-S. This starts the SDRAM clocks (SCLKs). The Self-Refresh Exit can be issued after the MRH-Ss are levelized.

4.2.13. System Clocking

The MRH-S receives the differential Direct RDRAM clock from the DRCG clock generator chip in the system. From this clock, the MRH-S generates two copies of SCLK for SDRAM use. A feedback input (SCLKFDBK) is provided on the MRH-S to connect to an output from the clock buffer for phase alignment.

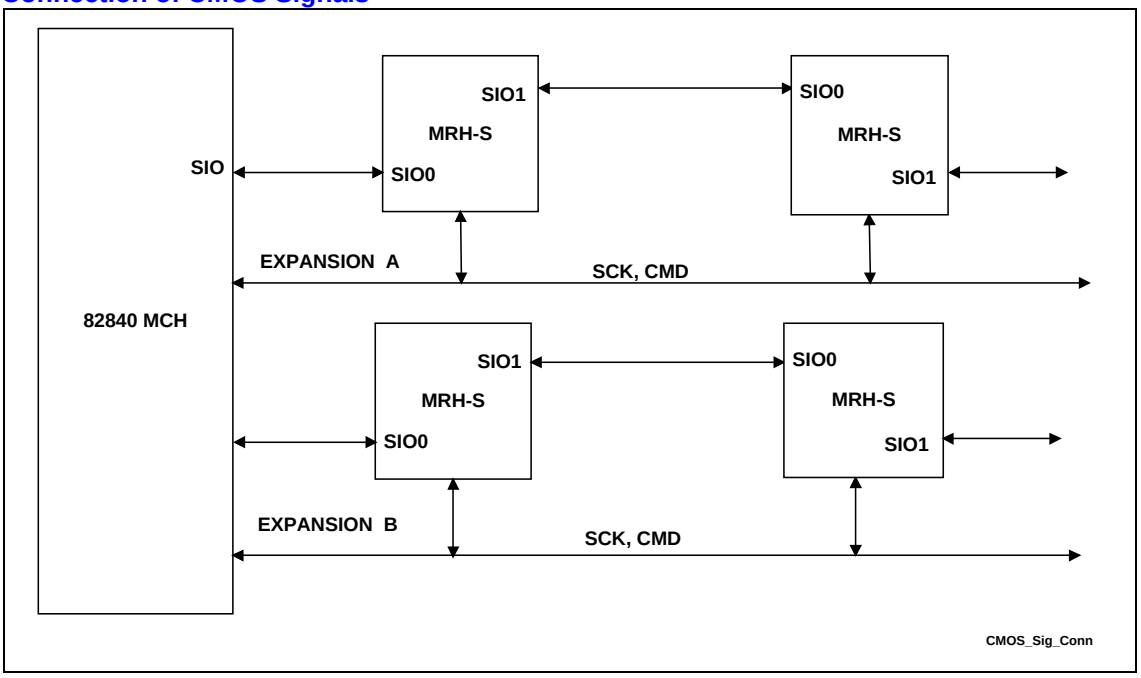
4.2.14. SDRAM Timing Parameters

The MRH-S needs to be aware of only one SDRAM timing parameter to operate properly. This timing parameter is CAS Latency (CL). All other SDRAM timing parameters are taken care of by the MCH. The MRH-S supports CAS latencies of 2 and 3.

4.3. CMOS Signal Protocol

The CMOS interface signals and protocol on the Direct RDRAM* Channel are used for MRH-S initialization and register accesses. The connection of Direct RDRAM CMOS signals between MCH and the MRH-S is illustrated in the Figure 4.

Figure 4. Connection of CMOS Signals



Using this interface, control packets are passed from the MCH to the MRH-S. The control packets may be directed to individual MRH-Ss or broadcasted to all MRH-Ss.

4.3.1. Serial Control Packet Formats

The serial control packets used on Direct RDRAM are described below. Four types of packets are defined:

- Direct RDRAM serial request packets—SRQ.
- Direct RDRAM serial address—SA.
- Direct RDRAM serial interval—SINT.
- Direct RDRAM serial data—SD.

The following figures show the layout of Register Read, Register Write, and Non-Register Operation packet types.

Figure 5. Direct RDRAM Serial Control Packet Format for Register Read

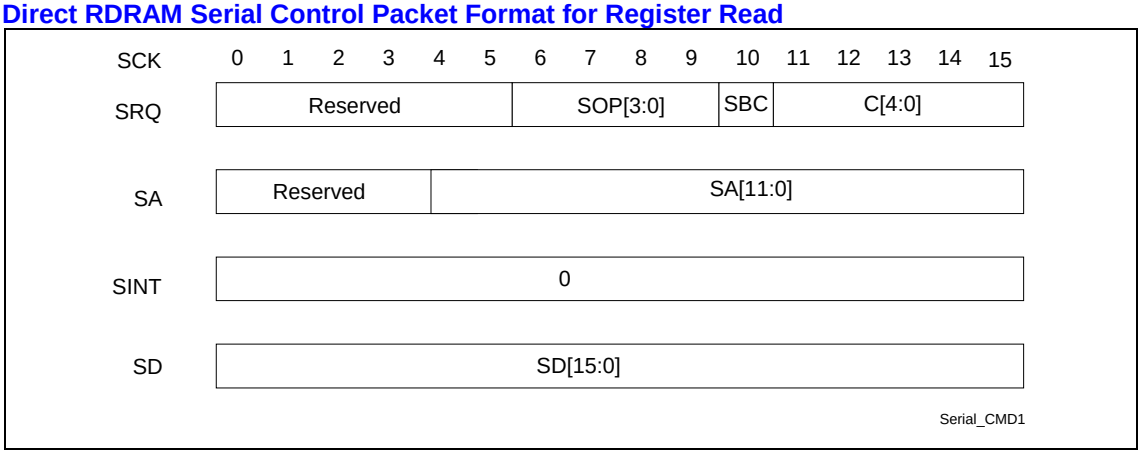


Figure 6. Direct RDRAM Serial Control Packet Format for Register Write

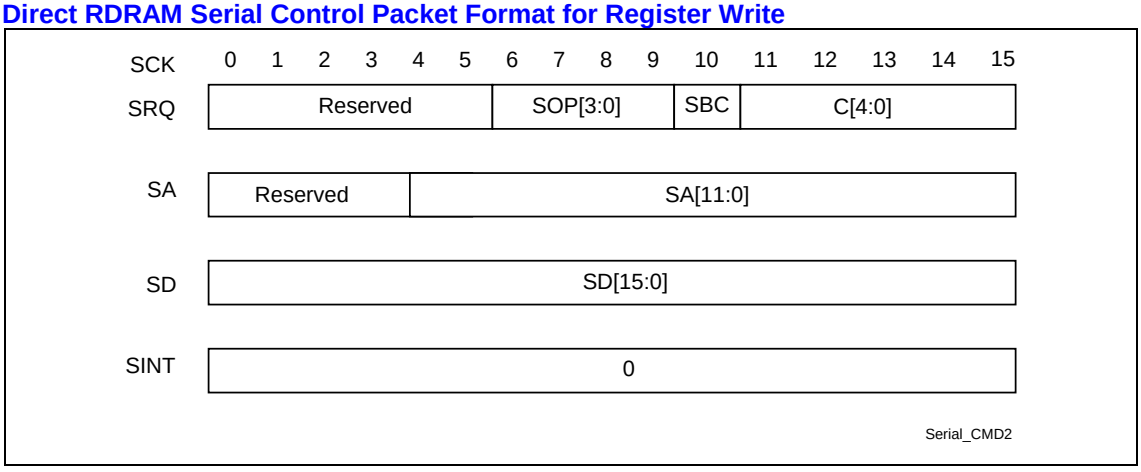
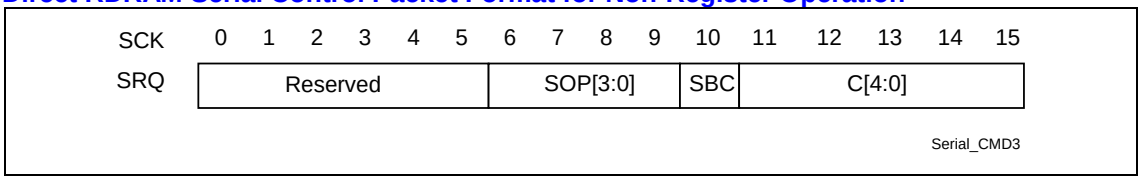


Figure 7. Direct RDRAM Serial Control Packet Format for Non-Register Operation



Note that these packet formats are the same as those used by the Direct RDRAM devices. Table 6 describes each of the fields for these serial packets.

Table 6. Direct RDRAM Serial Packet Field Definitions

Field	Description
SOP[3:0]	**Serial Op-code (SOP).** Specifies command for control register operations. **0000 = SRD:** Serial read of the register specified in SA[11:0] from MRH-S specified by C[4:0]. **0001 = SWR:** Serial write of the register specified in SA[11:0] from MRH-S specified by C[4:0]. All other combinations are reserved.
SBC	**Serial Broadcast:** 1 = All MRH-S's must execute the specified SOP command.
C[4:0]	**Serial Address:** Compared to bits [4:0] of the INIT register to select the MRH-S to which the Direct RDRAM serial transaction is directed to.
SA[11:0]	**Serial Register Address:** SA[11:0] selects which control register of the selected MRH-S is read or written.
SD[15:0]	**Serial Data:** The 16 bits of data read from or written to the selected control register in the selected MRH-S.

The following sections detail the available packet formats and the operations that can be performed on the serial control bus.

4.3.2. Transactions

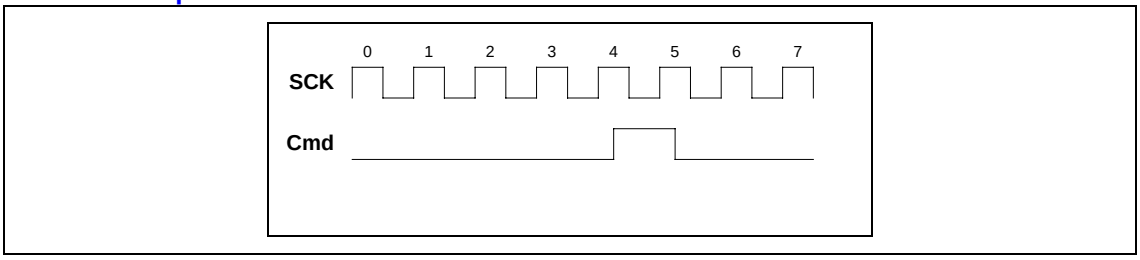
4.3.2.1. Reset

After power-on, the MRH-S's in the memory system must be reset. This process uses the following steps:

1. Reset the SIO chain that connects the MRH-Ss together.
2. Reset all MRH-Ss on the Direct RDRAM channel using serial control packets. At this point a register read can be issued to determine if the devices connected on the Direct RDRAM channel are MRH-Ss or other types of Direct RDRAM devices.

First, the SIO serial chain (SIO-SIO0-SIO1) is reset by issuing an SIO reset sequence as shown in Figure 8. CMD is sampled on both the rising and falling edges of SCK. A 1100 sequence on CMD resets the state machine that controls the SIO pins in each MRH-S. After this reset, the SIO pin is configured as an input and the SIO1 pin is configured as an output on every MRH-S. Also the SIO repeater bit in the MRH-S is set to 1.

Figure 8. SIO Reset Sequence



4.3.2.2. Register Operations

This section shows the serial read and write operations for control registers within the MRH-S. Figure 9 shows the control register read operation and Figure 10 shows the control register write operation.

Figure 9. Register Read

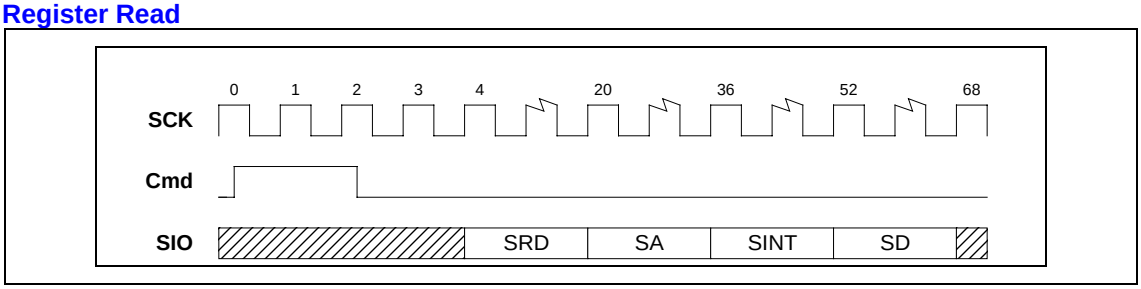
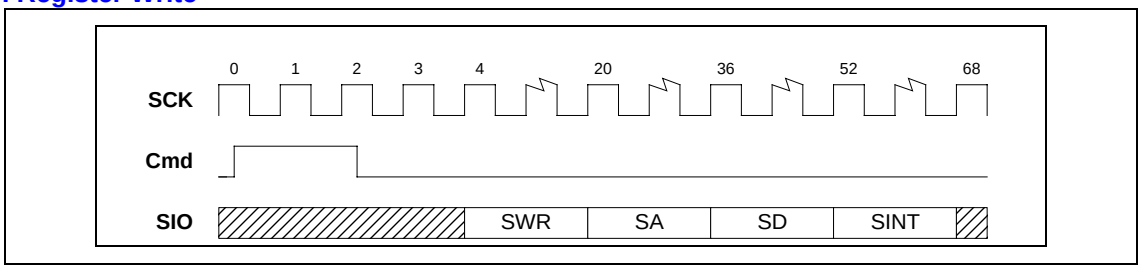


Figure 10. Register Write



5. Pinout and Package Information

5.1. MRH-S Ballout Assignment

The following figures show a top view of the MRH-S ballout. The table lists the ballout in alphabetical order by signal name.

Figure 11. MRH-S Ballout (Top View—Left Side)

	1	2	3	4	5	6	7	8	9
A	VSS	VSS	DQA8	DQA6	DQA2	DQA0	CFM	CTM#	RQ6
B	VSS	VCC2_5	VSS	VSS	DQA4	VSS	CFM#	CTM	VSS
C	VSS	VCC2_5	DQA7	DQA5	DQA3	DQA1	VSS	VSS	RQ7
D	DQM	VSS	VSS	VSS	VSS	VCC2_5	VSS	RAMREFA	RAMREFB
E	MD62	TESTIN#	MD63	VCC2_5	VCC2_5	VCC2_5	VCC2_5		VCC2_5
F	MD61	VSS	MD31	RST#	VCC3_3				
G	MD59	MD60	MD29	MD30	VCC3_3				
H	MD57	MD58	MD26	MD28				VSS	VSS
J	MD56	MD24	VSS	MD27	VCC3_3			VSS	VSS
K	MD55	MD23	MD22	MD25				VSS	VSS
L	MD53	MD21	MD54	MD20	VCC3_3				
M	MD51	MD52	VSS	MD19	VCC3_3				
N	MD18	CKE1	CKE3	MD17	VCC2_5	VCC3_3	VCC3_3		VCC3_3
P	MD16	MD49	MD50	CSA1#	CSB1#	MAA11	MAB11	MAA7	MAB7
R	SCLKB	VCC3_3	MD48	CSA2#	BAB0	BAA0	VSS	MAA8	MAB8
T	SCLKA	MECC7	MECC2	CSB2#	CKE0	BAB1	MAB12	MAA9	MAB9
U	VSS	SCLKFDBK	MECC6	MECC3	CKE2	BAA1	MAA12	MAA10	MAB10
	1	2	3	4	5	6	7	8	9

Figure 12. MRH-S Ballout (Top View—Right Side)

10	11	12	13	14	15	16	17	
RQ5	RQ2	RQ0	DQB3	DQB5	DQB7	SCK	CMD	A
RQ4	VSS	DQB1	VSS	DQB6	VSS	VSS	VCC1_8	B
RQ3	RQ1	DQB0	DQB2	DQB4	DQB8	SIO0	SIO1	C
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	D
	VCC2_5	VCC2_5	VCC2_5	MD0	MD1	MD33	MD32	E
			VCC3_3	MD2	MD3	MD35	MD34	F
			VCC3_3	MD4	MD5	VSS	MD36	G
VSS				MD6	MD7	MD38	MD37	H
VSS			VCC3_3	MD8	VSS	MD40	MD39	J
VSS				VSS	MD10	MD9	MD41	K
			VCC3_3	MD12	MD11	MD43	MD42	L
			VCC3_3	MD13	VSS	MD45	MD44	M
	VCC3_3	VCC3_3	VCC2_5	MD15	MD47	MD14	MD46	N
MAA6	MAB6	MAA0	MAB0	WEA#	CASA#	WEB#	CASB#	P
VSS	MAB5	MAA1	MAB1	MECC4	MECC0	VSS	MECC1	R
MAA5	MAA2	MAB2	VSS	MECC5	CSB3#	CSA3#	CSA0#	T
MAA4	MAB4	MAA3	MAB3	CSB0#	RASB#	RASA#	VSS	U
10	11	12	13	14	15	16	17	

Table 7. MRH-S Alphabetical Ballout List

Signal	Ball #
BAA0	R6
BAA1	U6
BAB0	R5
BAB1	T6
CASA#	P15
CASB#	P17
CFM	A7
CFM#	B7
CKE0	T5
CKE1	N2
CKE2	U5
CKE3	N3
CMD	A17
CSA0#	T17
CSA1#	P4
CSA2#	R4
CSA3#	T16
CSB0#	U14
CSB1#	P5
CSB2#	T4
CSB3#	T15
CTM	B8
CTM#	A8
DQA0	A6
DQA1	C6
DQA2	A5
DQA3	C5
DQA4	B5
DQA5	C4
DQA6	A4
DQA7	C3
DQA8	A3
DQB0	C12
DQB1	B12
DQB2	C13
DQB3	A13
DQB4	C14
DQB5	A14
DQB6	B14
DQB7	A15
DQB8	C15
DQM	D1
MAA0	P12
MAA1	R12
MAA2	T11
MAA3	U12
MAA4	U10
MAA5	T10
MAA6	P10
MAA7	P8
MAA8	R8
MAA9	T8
MAA10	U8
MAA11	P6
MAA12	U7
MAB0	P13
MAB1	R13
MAB2	T12
MAB3	U13
MAB4	U11
MAB5	R11
MAB6	P11
MAB7	P9
MAB8	R9
MAB9	T9
MAB10	U9
MAB11	P7
MAB12	T7
MECC0	R15
MECC1	R17
MECC2	T3
MECC3	U4
MECC4	R14
MECC5	T14
MECC6	U3
MECC7	T2
MD0	E14
MD1	E15
MD2	F14
MD3	F15
MD4	G14
MD5	G15
MD6	H14
MD7	H15
MD8	J14
MD9	K16
MD10	K15
MD11	L15
MD12	L14
MD13	M14
MD14	N16
MD15	N14
MD16	P1
MD17	N4
MD18	N1
MD19	M4
MD20	L4
MD21	L2
MD22	K3
MD23	K2
MD24	J2
MD25	K4
MD26	H3
MD27	J4
MD28	H4
MD29	G3
MD30	G4
MD31	F3
MD32	E17
MD33	E16
MD34	F17
MD35	F16
MD36	G17
MD37	H17
MD38	H16
MD39	J17
MD40	J16
MD41	K17
MD42	L17
MD43	L16
MD44	M17
MD45	M16
MD46	N17
MD47	N15
MD48	R3
MD49	P2
MD50	P3
MD51	M1
MD52	M2
MD53	L1
MD54	L3
MD55	K1
MD56	J1
MD57	H1
MD58	H2
MD59	G1
MD60	G2
MD61	F1
MD62	E1
MD63	E3

Signal	Ball #
RAMREFA	D8
RAMREFB	D9
RASA#	U16
RASB#	U15
RQ0	A12
RQ1	C11
RQ2	A11
RQ3	C10
RQ4	B10
RQ5	A10
RQ6	A9
RQ7	C9
RST#	F4
SCK	A16
SCLKA	T1
SCLKB	R1
SCLKFDBK	U2
SIO0	C16
SIO1	C17
TESTIN#	E2
VCC1_8	B17
VCC2_5	B2
VCC2_5	C2
VCC2_5	D6
VCC2_5	E4
VCC2_5	E5

Signal	Ball #
VCC2_5	E6
VCC2_5	E7
VCC2_5	E9
VCC2_5	E11
VCC2_5	E12
VCC2_5	E13
VCC2_5	N5
VCC2_5	N13
VCC3_3	F5
VCC3_3	F13
VCC3_3	G5
VCC3_3	G13
VCC3_3	J5
VCC3_3	J13
VCC3_3	L5
VCC3_3	L13
VCC3_3	M5
VCC3_3	M13
VCC3_3	N6
VCC3_3	N7
VCC3_3	N9
VCC3_3	N11
VCC3_3	N12
VCC3_3	R2
VSS	A1
VSS	A2

Signal	Ball #
VSS	B1
VSS	B3
VSS	B4
VSS	B6
VSS	B9
VSS	B11
VSS	B13
VSS	B15
VSS	B16
VSS	C1
VSS	C7
VSS	C8
VSS	D2
VSS	D3
VSS	D4
VSS	D5
VSS	D7
VSS	D10
VSS	D11
VSS	D12
VSS	D13
VSS	D14
VSS	D15
VSS	D16
VSS	D17
VSS	F2

Signal	Ball #
VSS	G16
VSS	H8
VSS	H9
VSS	H10
VSS	J3
VSS	J8
VSS	J9
VSS	J10
VSS	J15
VSS	K8
VSS	K9
VSS	K10
VSS	K14
VSS	M3
VSS	M15
VSS	R7
VSS	R10
VSS	R16
VSS	T13
VSS	U1
VSS	U17
WEA#	P14
WEB#	P16

5.2. MRH-S Package Dimension

This section shows the mechanical dimensions for the MRH-S device. The package is a 241 Ball Grid Array (BGA).

Figure 13. Package Dimensions (241 BGA) – Top and Side Views

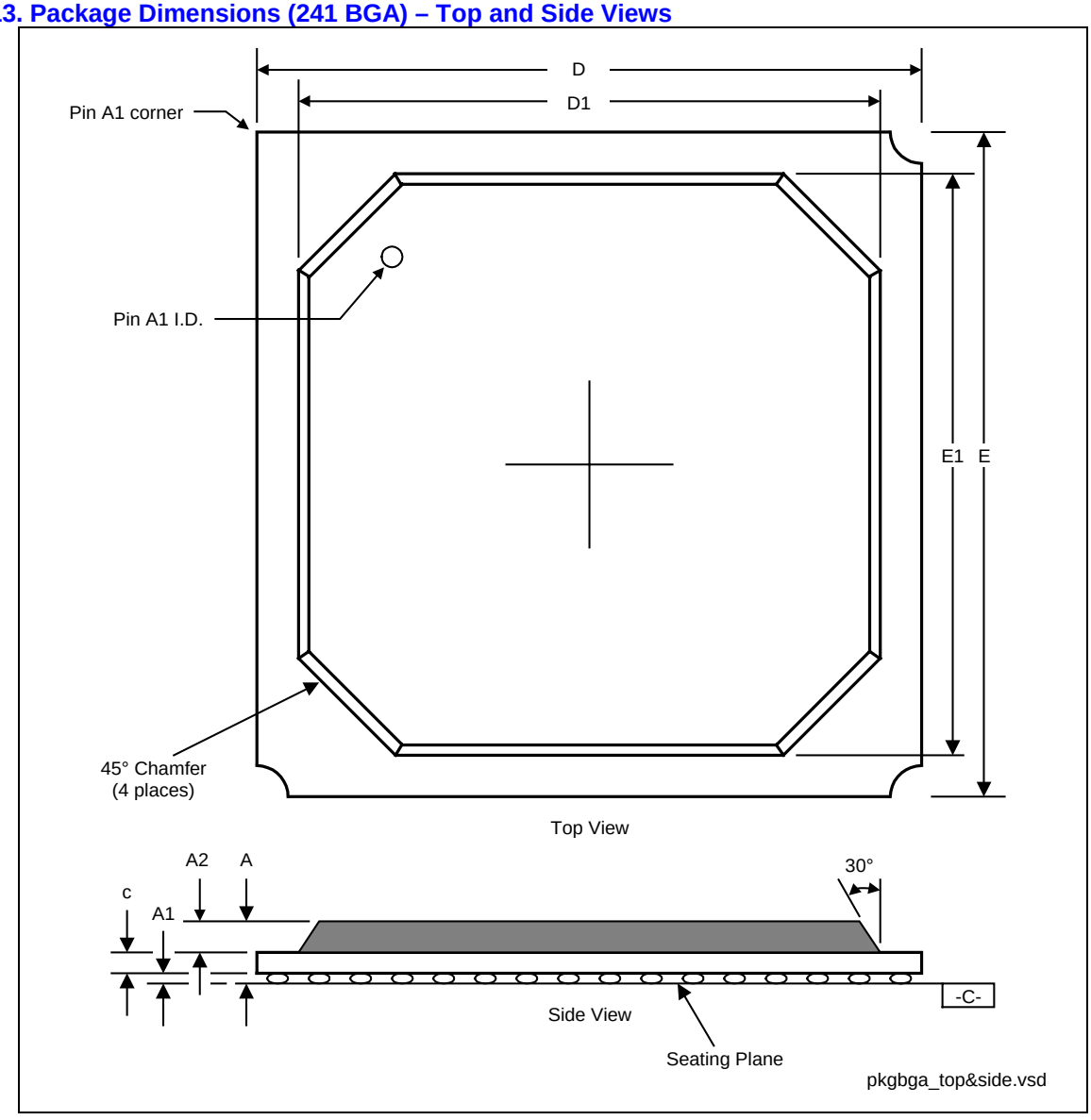


Figure 14. Package Dimensions (241 BGA) – Bottom View

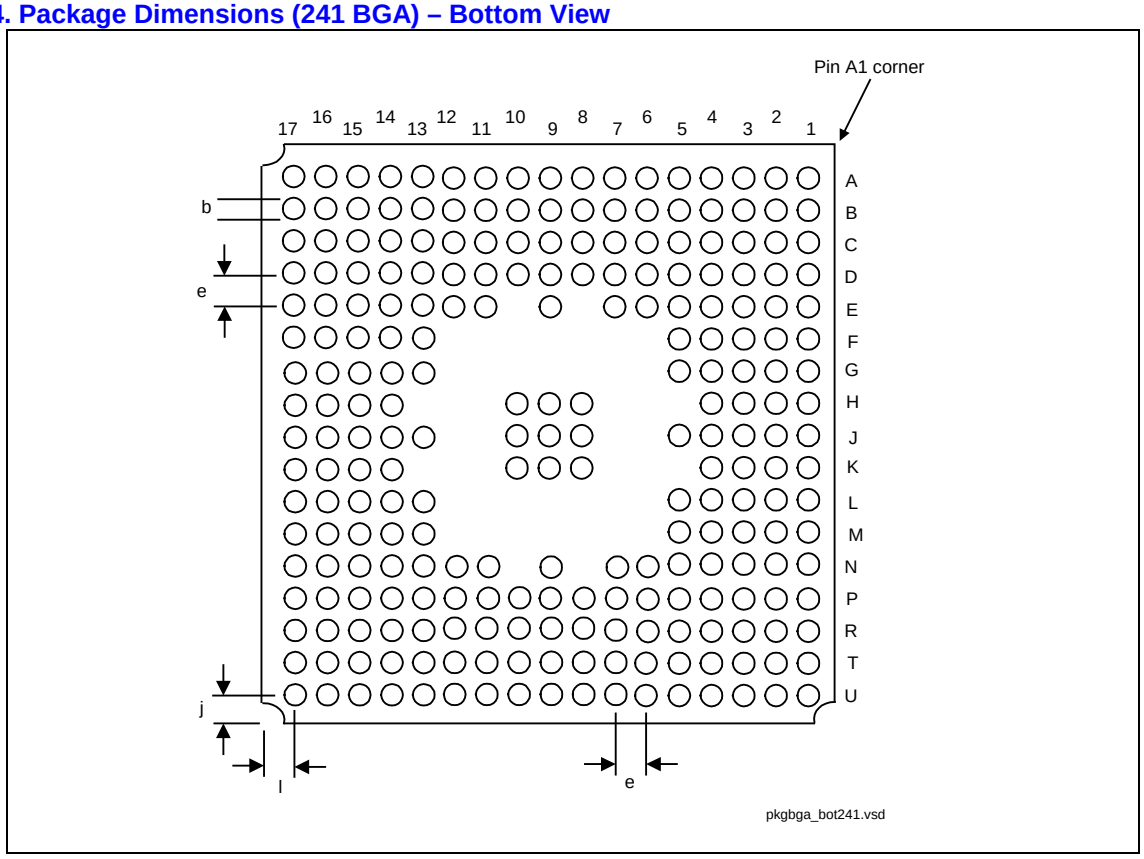


Table 8. BGA Package Dimensions (241 BGA)

Symbol	Min	Nominal	Max	Units	Note
A	2.19	2.38	2.57	mm	
A1	0.50	0.60	0.70	mm	
A2	1.12	1.17	1.22	mm	
D	22.80	23.00	23.20	mm	
D1	19.25	19.50	19.75	mm	
E	22.80	23.00	23.20	mm	
E1	19.25	19.50	19.75	mm	
e	1.27 (solder ball pitch)			mm	
l	1.34 REF.			mm	
J	1.34 REF.			mm	
M	17 x 17 Matrix			mm	
b^2	0.60	0.75	0.90	mm	
c	0.57	0.61	0.65	mm	

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5-1982
2. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-)
3. Primary Datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

5.3. RSL Normalized Trace Length Data

These lengths must be considered when matching trace lengths as described in the design guide. Note that these lengths are normalized to 0 with the longest trace on the package. They do not represent the actual lengths from pad to ball.

The following formula is used to determine ΔL_{PCB} :

$$\Delta L_{PCB} = (\Delta L_{pkg} * Vpkg) / V_{PCB}$$

ΔL_{PCB} is the nominal Δ PCB trace length to be added on the PCB

ΔL_{Pkg} is the nominal Δ package trace length

V_{pkg} is the package trace velocity, and the nominal value is 180 ps/in

V_{PCB} is the PCB trace velocity

The data given can be re-normalized to start routing from a different ball. If a different RSL signal (other than longest trace) is used for the nominalization, simply use the following equation:

$$\text{New } \Delta L_{pkg}' = \Delta L_{pkg} - \Delta L_{RSL}$$

ΔL_{pkg} is the nominal Δ package trace length

ΔL_{rsl} is the RSL signal used for re-normalization

For example: For the MCH, if MCH CHA_CFM trace length is used for nominalization, then:

	ΔL_{pkg} (mils)	New ΔL_{pkg}' (mils)
CHA_CF	102.756	0.000
CHA_CFM	118.897	6.142
CHA_CT	130.315	27.559
:	:	:
:	:	:
CHA_RQ7	175.984	73.228

Table 9. MRH-S RSL Normalized Trace Length Data

ΔL_{Pkg} Normalized to DQA6

Signal	Ball	ΔLPKG (mils)
CTM	B8	95.673
CTM#	A8	104.023
CFM	A7	91.441
CFM#	B7	83.331
DQA0	A6	42.276
DQA1	C6	181.027
DQA2	A5	28.213
DQA3	C5	114.031
DQA4	B5	70.677
DQA5	C4	87.311
DQA6	A4	0.000
DQA7	C3	96.138
DQA8	A3	5.854
DQB0	C12	139.905
DQB1	B12	87.189

ΔL_{Pkg} Normalized to DQA6 (cont)

Signal	Ball	ΔLPKG (mils)
DQB2	C13	114.413
DQB3	A13	68.311
DQB4	C14	80.401
DQB5	A14	52.106
DQB6	B14	31.350
DQB7	A15	5.713
DQB8	C15	48.142
RQ0	A12	30.102
RQ1	C11	147.704
RQ2	A11	94.543
RQ3	C10	160.523
RQ4	B10	112.437
RQ5	A10	49.929
RQ6	A9	38.118
RQ7	C9	164.437

6. Testability

The MRH-S supports the following test modes:

Number of Clocks[SCLKFDBK] TESTIN# Driven Low	Test Mode
<5	**Reserved. Do Not Attempt**
6	All 'Z'
7	Non-RAC NAND Chain
8-39	**Reserved. Do Not Attempt**
40	RAC XOR Chain

6.1. Tri-state Mode

The tri-state test mode is activated by asserting the TESTIN# signal low for 6 clocks [SCLKFDBK]. All outputs and bi-directional pins are tri-stated, including the NAND tree and XOR tree outputs.

6.2. NAND Tree Test Mode

6.2.1. SDRAM Interface Only

The MRH-S has 3 NAND chains implemented for all non-RAC pins. This test mode activates by asserting the TESTIN# signal low for 7 clocks (SCLKFDBK). This test mode can be used to check the connectivity of the pins.

Table 10. NAND CHAIN #1

Name	Ball	Chain Element #	Note
MD_63	E3	0	
MD_31	F3	1	
DQMIN	D1	2	
MD_62	E1	3	
MD_30	G4	4	
MD_60	G2	5	
MD_61	F1	6	
MD_28	H4	7	
MD_29	G1	8	
MD_59	G3	9	
MD_58	H2	10	
MD_26	H3	11	
MD_57	H1	12	
MD_27	J4	13	
MD_24	J2	14	
MD_56	J1	15	
MD_55	K1	16	
MD_22	K3	17	
MD_23	K2	18	
MD_53	L1	19	
MD_21	L2	20	
MD_25	K4	21	
MD_54	L3	22	
MD_20	L4	23	
MD_51	M1	24	
MD_52	M2	25	
MD_18	P1	26	
MD_16	N1	27	
CKE_1	N2	28	
MD_49	P2	29	
MD_19	M4	30	
SCLKB	R1	31	
CKE_3	N3	32	
MD_50	P3	33	

Table 10. NAND CHAIN #1

Name	Ball	Chain Element #	Note
SCLKA	T1	34	
MD_17	N4	35	
DQM_7	T2	36	
CMD	A17		Output

Table 11. NAND CHAIN #2

Name	Ball	Chain Element #	Note
MD_48	R3	0	
CSAB_1	P4	1	
CSAB_2	R4	2	
CSBB_1	P5	3	
DQM_2	T3	4	
BAB_0	R5	5	
MAA_11	P6	6	
CSBB_2	T4	7	
CKE_0	T5	8	
DQM_6	U3	9	
BAA_0	R6	10	
DQM_3	U4	11	
BAB_1	T6	12	
CKE_2	U5	13	
BAA_1	U6	14	
MAB_11	P7	15	
MAA_7	P8	16	
MAB_12	T7	17	
MAA_12	U7	18	
MAA_9	T8	19	
MAA_8	R8	20	
MAA_10	U8	21	
MAB_10	U9	22	
MAB_7	P9	23	
MAB_9	T9	24	
MAB_8	R9	25	

Table 11. NAND CHAIN #2

Name	Ball	Chain Element #	Note
MAA_4	U10	26	
MAA_5	T10	27	
MAB_4	U11	28	
MAA_2	T11	29	
MAA_6	P10	30	
MAA_3	U12	31	
MAB_5	R11	32	
MAB_6	P11	33	
MAB_2	T12	34	
MAB_3	U13	35	
CSBB_0	U14	36	
MAA_1	R12	37	
DQM_5	T14	38	
RASBB	U15	39	
MAA_0	P12	40	
MAB_1	R13	41	
RASAB	U16	42	
CSBB_3	T15	43	
CSAB_3	T16	44	
DQM_4	R14	45	
DQM_0	R15	46	
MAB_0	P13	47	
SIO0	C16		Output

Table 12. NAND CHAIN #3

Name	Ball	Chain Element #	Note
WEAB	P14	0	
CASAB	P15	1	
MD_15	N14	2	
MD_13	M14	3	
CSAB_0	T17	4	
WEBB	P16	5	
MD_47	N15	6	
DQM_1	R17	7	

Table 12. NAND CHAIN #3

Name	Ball	Chain Element #	Note
MD_14	N16	8	
CASBB	P17	9	
MD_46	N17	10	
MD_45	M16	11	
MD_12	L14	12	
MD_44	M17	13	
MD_11	L15	14	
MD_43	L16	15	
MD_42	L17	16	
MD_10	K15	17	
MD_9	K16	18	
MD_41	K17	19	
MD_8	J14	20	
MD_40	J16	21	
MD_39	J17	22	
MD_37	H17	23	
MD_38	H16	24	
MD_36	G17	25	
MD_7	H15	26	
MD_34	F17	27	
MD_6	H14	28	
MD_35	F16	29	
MD_4	G14	30	
MD_5	G15	31	
MD_32	E17	32	
MD_33	E16	33	
MD_3	F15	34	
MD_2	F14	35	
MD_1	E15	36	
SIO0	C16	37	
SCK	A16	38	
MD_0	E14	39	
SIO1	C17		Output

6.2.2. RAC Interface XOR Tree

The MRH-S utilizes the following RAC XOR chain to check for connectivity on its Direct RDRAM channel. This test mode activates by asserting the TESTIN# signal low for 40 clocks (SCLKFDBK).

Table 13: RAC XOR Chain Mapping

ELEMENT Number	Associated Pin Number
0	DQA8
1	DQA7
2	DQA6
3	DQA5
4	DQA4
5	DQA3
6	DQA2
7	DQA1
8	DQA0
9	CTM
10	CTM#
11	CFM#
12	CFM
13	RQ6
14	RQ7
15	RQ5
16	RQ4
17	RQ3
18	RQ2
19	RQ1
20	RQ0
21	DQB1
22	DQB3
23	DQB0
24	DQB2
25	DQB5
26	DQB4
27	DQB6
28	DQB7
29	DQB8
	Output on CMD signal

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